Siliconpolitik v2025

Challenges and Opportunities for India-Japan Semiconductor Collaboration

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The Big Picture

There are several high-complementarity and high-feasibility areas of semiconductor collaboration between India and Japan.

The Story of the Past

1. All top-25 fabless companies by revenue have design centres in India[1]
   1.1 Indian value addition is under-counted because of HQ-based data. PaxSilica or not, India will remain a major node.
2. Zero commercial CMOS fabrication capabilities
   2.1 Research and small-volume capacity for defence and strategic needs exists
3. Insignificant testing and packaging presence thus far
4. Specialised gases and materials firms present in adjacent sectors

[1] Ezell, Stephen. Assessing India's Readiness to Assume a Greater Role in Global Semiconductor Value Chains. 2024. https://itif.org/publications/2024/02/14/india-semiconductor-readiness/.

What's Different this Time

- Upfront capital support
- Collaboration between state and union governments
- Efforts across the entire value chain
- Internalising "Metacriticality"

Approved and Under Construction Projects (as of Sep 2025)

- 1 CMOS Chip Fabrication plant ($<$10% of India's demand)
- 1 Compound Semiconductor fabrication and packaging plant
- 8 Assembly, Test and Packaging plants
- Chip design projects from 23 companies approved under P-DLI scheme with a total project cost of $\sim$ 700 crore (goal is to support 100 start-ups in their go-to-market strategy by Dec 2026).

Likely: Mature Nodes Overcapacity

- 107 new fabs are set to come up by 2030; 91 already work in progress
- Mature nodes segment highly likely to face overcapacity and 'China Shock'
- Demand for advanced fab nodes likely to sustain
- Driven by national security concerns not market demand
- Implication: mature node fabs need anchor customers. Trusted Foundry Accreditation will help.

Blackswan: A Taiwan Blockade or Invasion will rock the Industry

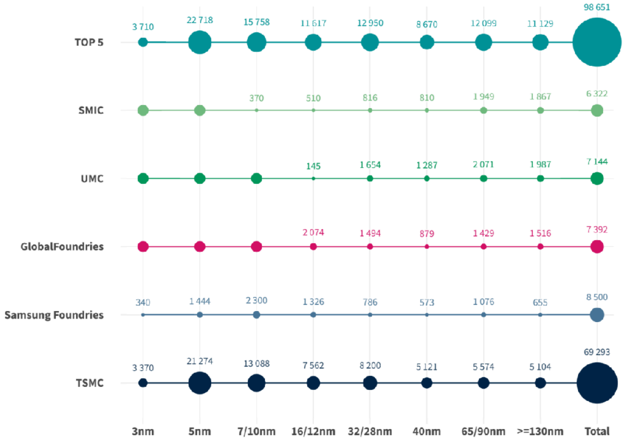

Figure 1: source: Gartner and Crédit Agricole S.A.

Blackswan: A Taiwan Blockade or Invasion will rock the Semiconductor Industry

- TSMC and UMC have significant presence in advanced *and* mature nodes
- Invasion or blockade will lead to shortages for at least two-three years
- Implication 1: Flexible sovereign funds needed to support domestic firms and start-ups in case of this eventuality
- Implication 2: Aggregate demand from domestic players and encourage them to work with foundries outside Taiwan

Highly Likely: Global Talent Shortage

- global shortage of *fab process engineers* and *experienced technicians* is the single biggest bottleneck to all national chip ambitions.
- Implication: need focus on talent development in these segments. Scope for collaboration between India and Japan.

Likely: More Restrictions and Controls

Strategic Objective	Instruments Used	Underrated Repercussions
Denial	Sanctions and controls	Difficult to sustain; incentives for backroom deals with adversary
	Restricting movements of semiconductor labour	Can slow down technical progress
	End-use restrictions	Encourages adversary to build local capacity in a focused manner
	Investment screening	Can slow down technical progress
Outpace adversary	industrial espionage to steal secrets, targeted poaching	Invites stricter controls on professionals from the stealing country
	Build partnerships	Self-sufficiency is a myth
	Indigenisation and industrial policy	Difficult to sustain
	Economic coercion	Self-damage
	Encouraging the movement of labour	Human capital is the dark horse in the race for semiconductor supremacy
	Increase dependence and control	Helps manage the adversary's pace to an extent
Increase supply chain resilience	Promote open-source hardware	Still a nascent field
	Mapping supply chains	Firms care more about resilience than governments
	Build partnerships to create a resilient supply chain.	Self-sufficiency is a myth.
Influence minds and actions	Hardware espionage	Limited impact on national power

Figure 2: Source: Author

Implication for Japan and India Given the Restrictions

- Forge an Open Tech Maitri geared towards digital strategic autonomy
- fund moonshot projects to create open Graphics Processing Unit (GPU) architecture projects like Libre-SOC
- identify, support and build global open source alternatives for EDA software and processor IPs

Packaging Becomes Cool

- The game is shifting from the "Fab" (Front-End) to the "OSAT" (Back-End).
- "System-in-Package" (SiP) allows mix-and-match of small chips ("chiplets") from different fabs (e.g., 3nm AI + 22nm I/O + 65nm Power).
- Advanced Packaging is now strategically important
- Implication: Develop OSAT as leverage. Partnerships in outsourced assembly and test (OSAT) would support complementary initiatives and investment in either country.

Semiconductor Manufacturing Equipment is a Complementary Fit

- Japan's strengths: semiconductor manufacturing equipment (Tokyo Electron, SCREEN), critical chemicals/photoresists (JSR, Shin-Etsu)
- India's ISM2.0 hopes to build on these auxiliary segments of the supply chain.
- Japan's leadership in Nano Imprint Lithography is likely to find interest in India as it builds new processes afresh.

Master the Niche

- For defence, Compound Semiconductors like GaN are more important than cutting-edge silicon.
- Gallium Nitride (GaN) is the material for AESA Radars and Electronic Warfare.
- Implications: Long-term contracts, trusted foundry accreditation, buyer of first resort

Unlocking India's Strengths in the Fabless Segment

- joint commercial projects for semiconductors, including in such emerging areas as chiplets, can harness complementary strengths.
- Renesas' acquisition of Steradian Semiconductors (a 4D imaging radar solution company) in 2022 is an example of a successful exit for an Indian hardware start-up.
- a dedicated India-Japan research academy focused on very large-scale integration design and new semiconductor materials could help drive innovation.